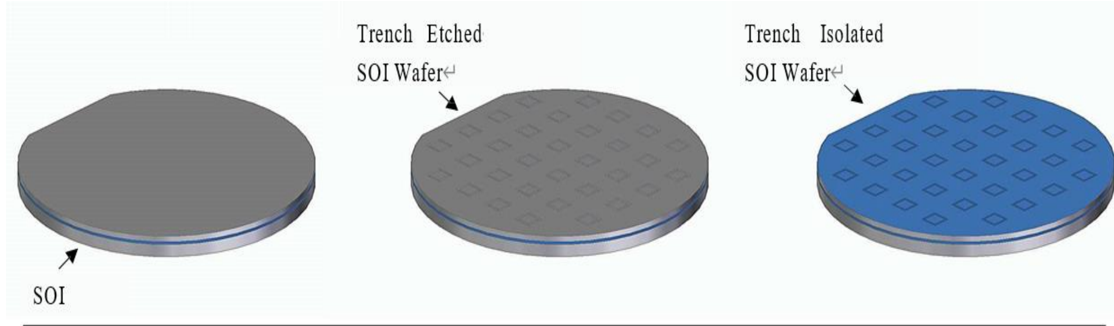
厚 膜 深 沟 蚀 刻 绝 缘 体 上 硅
TSOI Solutions



我司能够提供 4-6 英寸厚膜深沟腐蚀 SOI 晶片。该类 SOI 晶片使用了厚膜 SOI 技术，最先进的高纵横比深沟槽蚀刻及氧化物/聚填充而得以实现。这是一种介电隔离技术，使同一芯片上的各组件之间形成高压隔离。它的好处有：可消除埋层、epi 层及 P+隔离扩散，最小化寄生电容，高质量硅晶体层，增加可得芯片数，高电压击穿能力。

我们可以按客户提供的掩模板加工蚀刻介质隔离基片，或为客户提供完整的后道介质隔离集成电路加工，还可以根据客户来图进行设计和加工。我们可提供的后道技术包括：双级、CMOS 和 BiCMOS。

BonTek presents its dielectric isolation technology – delivering high voltage isolation between components on the same chip. Isolation is achieved using thick film SOI technology combined with state-of-the-art high aspect ratio deep trench etching and oxide/poly refill. This technology is available on all wafer sizes from 100mm to 150mm and silicon device layers from 1.5um to 100um.

Supply Options Available:

- Provision of DI Substrate from isolation mask provided.
- Provision of Fully processed DI IC using BonTek as foundry to complete post isolation processing.
- Provision of Full IC design and fabrication on DI from customer schematic.

Post Isolation technologies available:

- Simple Bipolar
- CMOS (1P, 2M)
- BiCMOS (1P, 2M)

加工能力 processing capacity

Parameter 参数	Specification Range 尺寸规格范围
Wafer Diameter 直径	100, 125, 150 mm
Handle Layer Specifications 衬底层规格	
Handle Thickness 衬底层厚度	350–800 µm
Handle Thickness Tolerance 厚度公差	±5 µm
Stack Thickness 板叠厚度	350–1150 µm
Dopant Type 掺杂剂类型	N or P
Doping 掺杂	N type: Phos, Red Phos, Sb & As P type: Boron
Resistivity 电阻率	≤0.001 – ≥10000 Ω-cm
Growth Method 生长方式	CZ, MCZ or FZ
Crystal Orientation 晶体定向	<100>, <111> or <110>

Backside Finish 背面处理	Lapped/Etched or Polished
Buried Oxide Specifications 氧化物埋层规格	
Thermally Oxidised Buried Oxide Thickness 热氧化埋层厚度	0.2 – 4.0 µm grown on Handle, Device or both wafers
Device Layer Specifications 顶层规格	
Device Layer Thickness 顶层厚度	1.5 - 100 µm
Tolerance 公差	± 0.5 µm
Dopant Type 掺杂剂类型	N or P
Doping 掺杂	N type: Phos, Red Phos, Sb & As P type: Boron
Resistivity 电阻率	≤0.001 – ≥10000 Ω-cm
Growth Method 生长方式	CZ, MCZ or FZ
Crystal Orientation 晶体定向	<100>, <111> or <110>
Buried Layer Implant 埋层植入	N type or P type
Trench Mask Tone 槽腐蚀掩膜极性	Positive Resist
Trench Mask Type 槽腐蚀掩膜类型	E-beam master for projection aligner
Trench Line Width 沟线宽	> 2um
Trench Aspect Ratio 沟纵横比	15:1
Trench Sidewall Doping Type 沟槽侧壁掺杂型	Phosphorus
Trench Refill – Oxide (each sidewall) 沟槽填充 — 氧化物	0.1 – 1.0 µm
Trench Refill – Polysilicon 沟槽填充 — 多晶硅	To Fill (Doped or undoped Polysilicon)
Planarisation 磨平	CMP
Final Field Oxide 最终氧化	Thermal oxide + TEOS up to 1um

Applications 应用方向:

MEMS devices 微机电设备
Solid State Relay photovoltaic generators 固态继电器光伏发电机
Photovoltaic cells and Optoelectronic devices/ICs 光伏电池和光电子器件/集成电路
High Voltage Analog ICs for telecommunications 电信用高压模拟集成电路
High performance bipolar circuits 高性能双极电路
Smart Power ICs Integrated Sensors 智能电源集成电路传感器

Key Features 主要特征:

Complete device isolation 完全的设备层隔离
Significant die shrinkage compared with conventional Junction isolation 显著的芯片尺寸收缩
Much lower defect density than conventional DI technologies 缺陷密度比传统的 DI 技术低得多
Lower Substrate capacitance than bulk 更低电容
Lower cost than trench isolation on epi 更低成本

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